**Components documentation**

**Common components**

Register (in Register file)

Entity name: Reg

Inputs:

* Rst (1 bit)
* Clk (1 bit)
* Enable (1 bit)
* RegInput (32 bits)

Outputs:

* RegOutput (32 bits)

**Decode Stage components**

Register File

Entity name: RegFile

Inputs:

* Rst (1 bit)
* Clk (1 bit)
* WriteAddress (3 bits)
* ReadAddress1 (3 bits)
* ReadAddress2 (3 bits)
* WriteData (32 bits)
* readEnable (1 bit)
* writeEnable (1 bit)

Outputs:

* ReadData1 (32 bits)
* ReadData2 (32 bits)

**Execute Stage components**

ALU

Description:

* ALU instructions
  + NOT
  + INC
  + ADD
  + SUB
  + AND

Entity name: ALU

Inputs:

* Rst (1 bit)
* Clk (1 bit)
* WriteAddress (3 bits)
* ReadAddress1 (3 bits)
* ReadAddress2 (3 bits)
* WriteData (32 bits)
* readEnable (1 bit)
* writeEnable (1 bit)

Outputs:

* ReadData1 (32 bits)
* ReadData2 (32 bits)
* Instruction is 32 bits
* Opcode is 5 bits
* 8 registers (R0 -> R7)
* 2 special registers: PC + SP
* Each register is 32 bits
* Flag register (CCR) (4 bits)
  + Z (Zero flag)
  + N (Negative flag)
  + C (Carry flag)
* Control Signals:
  + Write Back Signal (whether we write back or not) (0: No WB, 1: WB)
  + Write Back from ALU or Memory (0: ALU, 1: Memory)
  + Branch (whether there is branch or not) (0: No branch, 1: Branch)
  + Type of branch (00: JMP, 01: JZ, 10: JN, 11: JC)
  + Execute 2nd operand from register or from immediate value (0: register, 1: immediate value)
  + Memory Write/Read (0 for write, 1 for read), (all instructions that don’t use memory will have a read signal)
  + SP Control:
    - Control unit outputs a signal that has 3 combinations:
      * 00: No change (false enable)
      * 01: +1 for POP and RET
      * 10: -1 for PUSH and CALL
* Forwarding Unit:
  + Inputs:
    - Write Address from ALU Buffer
    - Write Address from Memory Buffer
    - Current Read Address (Rsrc1 and Rsrc2) from Instruction Fetch
    - //should be address in buffer after decode since if second instruction is waiting for data in alu, it has to wait tell it reaches buffer after alu and in this case the second instruction will have reached buffer after decode
  + Output:
    - Selection line of MUX before Decode Buffers
      * Most significant 2 bits for data 1 and least significant 2 bits for data 2
      * 00 -> From register file
      * 01 -> From ALU
      * 10 -> From Memory
      * Ex:
        + 0000: Read Data 1 from register and Read Data 2 from register file
        + 0001: Read Data 1 from register file and Read Data 2 from ALU
        + 1010: Read Data 1 from Memory and Read Data 2 from Memory
        + 0100: Read Data 1 from ALU and read data 2 from register file
        + 1001: Read Data 1 from Memory and read Data 2 from ALU
  + Logic:
    - Compare Read Addresses 1 & 2 with Write Address from ALU and from memory Buffers

Alu:

* Input:
  + First register address which is the source register from ID/EX buffer
  + second input is out of mux
    - the selection of the mux depends on the instruction
    - if instruction is R-type or branch then the output of the mux is the second register read in decode stage
    - if the instruction is load/store or any instruction using immediate value then the sign extended immediate value is the output of mux
* output:
  + In R-type instruction, the output is the value that will be stored in the destination register and which will also be used in forwarding if needed
  + In load/store instruction the output is the address that will be used in memory stage to load or store
  + In branch instruction the output is the result of comparison which tells us whether to take the branch or not
  + Static Branch Prediction
    - Always not taken to minimize error.
    - Execute successor instruction in sequence.
    - Discard (flush) instructions in pipeline if branch was actually taken.